

Appl. No. 10/709,569
Amdt. dated November 30, 2004
Reply to Office action of August 31, 2004

Amendments to the Claims:

Listing of Claims:

Claim 1 (currently amended): A bipolar junction transistor, comprising:

- 5 a substrate;
 a dielectric layer formed on the substrate;
 an opening formed in the dielectric layer to expose a portion of the
substrate;
 a selective implant collector region formed in the substrate and
10 beneath the opening;
 a heavily doped polysilicon layer formed on a sidewall of the
opening to define a self-aligned base region in the opening;
 an intrinsic base doped region positioned in a bottom of the opening
and within the self-aligned base region defined by the heavily doped
15 polysilicon layer;
 a spacer formed on the heavily doped polysilicon layer to define a
self-aligned emitter region in the opening; and
 an emitter conductivity layer being filled within the self-aligned
emitter region, and a PN junction being formed between the emitter
20 conductivity layer and the intrinsic base doped region.

Claim 2 (original): The bipolar junction transistor of claim 1, wherein the
heavily doped polysilicon layer comprises a boron dopant with a dosage
ranging from $1\text{E}19$ to $1\text{E}21$ atoms/cm².

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Claim 3 (original): The bipolar junction transistor of claim 1, wherein the substrate is a silicon substrate.

5 Claim 4 (original): The bipolar junction transistor of claim 1, wherein the substrate is a non-selective epitaxial silicon substrate.

Claim 5 (original): The bipolar junction transistor of claim 1, further comprising a salicide layer formed on the emitter conductivity layer.

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Claim 6 (canceled)

Claim 7 (original): The bipolar junction transistor of claim 1, further comprising an extended conductivity layer formed on the dielectric layer
15 to connect to the heavily doped polysilicon layer.

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Claim 8 (original): The bipolar junction transistor of claim 7, further comprising an oxide layer and a silicon nitride layer formed between the extended conductivity layer and the dielectric layer.

Claim 9 (original): The bipolar junction transistor of claim 7, wherein the extended conductivity layer is composed of in-situ doped polysilicon.

Claim 10 (original): The bipolar junction transistor of claim 7, further
25 comprising a salicide layer formed on the extended conductivity layer.

Claim 11 (original): The bipolar junction transistor of claim 1, wherein

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the substrate further comprises at least a deep isolation trench.

Claim 12 (original): The bipolar junction transistor of claim 11, wherein
the substrate further comprises at least a channel stop region formed in
5 the bottom of the deep isolation trench.

Claim 13 (original): The bipolar junction transistor of claim 1, wherein
the intrinsic base doped region comprises a boron dopant.

- 10 Claim 14 (currently amended): A bipolar junction transistor, comprising:
a substrate;
at least a deep isolation trench formed in the substrate and at least a
channel stop region formed in the bottom of the deep isolation trench;
a dielectric layer formed on the substrate;
15 an opening formed in the dielectric layer to expose a portion of the
substrate;
a doped polysilicon layer formed on a sidewall of the opening and on
the dielectric layer outside of the opening, the doped polysilicon layer
defining a self-aligned base region in the opening;
20 an intrinsic base doped region positioned in a bottom of the opening
and within the self-aligned base region defined by the doped polysilicon
layer;
a spacer formed on the doped polysilicon layer to define a
self-aligned emitter region in the opening; and
25 an emitter conductivity layer being filled within the self-aligned
emitter region, and a PN junction being formed between the emitter
conductivity layer and the intrinsic base doped region.

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Claim 15 (original): The bipolar junction transistor of claim 14, wherein the doped polysilicon layer comprises a boron dopant.

- 5 Claim 16 (original): The bipolar junction transistor of claim 14, further comprising a salicide layer formed on the emitter conductivity layer and on the portion of the doped polysilicon layer outside of the opening.

- 10 Claim 17 (original): The bipolar junction transistor of claim 14, further comprising a selective implant collector (SIC) region formed in the substrate beneath the intrinsic base doped region.

Claim 18 (canceled)

- 15 Claim 19 (canceled)

Claim 20 (original): The bipolar junction transistor of claim 14, wherein the intrinsic base doped region comprises a boron dopant.

- 20 Claim 21 (new): A bipolar junction transistor, comprising:
a substrate;
at least a deep isolation trench formed in the substrate and at least a channel stop region formed in the bottom of the deep isolation trench;
a dielectric layer formed on the substrate;
25 an opening formed in the dielectric layer to expose a portion of the substrate;
a heavily doped polysilicon layer formed on a sidewall of the

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opening to define a self-aligned base region in the opening;

an intrinsic base doped region positioned in a bottom of the opening and within the self-aligned base region defined by the heavily doped polysilicon layer;

5 a spacer formed on the heavily doped polysilicon layer to define a self-aligned emitter region in the opening; and

an emitter conductivity layer being filled within the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the intrinsic base doped region.

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